Remarks

In the Office Action mailed March 23, 2004:

1. The abstract was objected to;
2. Claims 4, 11 and 12 were objected to, due to informalities;
3. Claim 3 was rejected under 35 U.S.C. § 112 ¶ 2;
4. Claims 1, 7, 8, 14 and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,202,975 (Rasbold);
5. Claims 2, 3, 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rasbold, in view of U.S. Patent No. 5,881,315 (Cohen);
6. Claims 4, 5, 11, 12, 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rasbold, in view of U.S. Patent No. 5,377,336 (Eickmeyer); and
7. Claims 6, 13 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rasbold, in view of U.S. Patent No. 5,941,983 (Gupta).

I. Abstract

The Abstract is amended as shown above.

II. Claim Informalities

Claims 4, 11 and 12 have been amended to correct the noted informalities.

III. Rejection under 35 U.S.C. § 112 ¶ 2

Claim 3 was cancelled.

IV. Rasbold (U.S. Patent No. 5,202,975)

Rasbold is directed to a method for scheduling instructions for a processor, wherein the instructions are reordered in response to a simulation of a run-time environment (column 4, lines 3-7. In particular, after a Leader Set of instructions is assembled, instructions to place in a Ready Set are determined through a compile-time simulation (column 8, lines 19-21).

A Desired Issue Time (DIT) is computed for the Leader Set instructions, and instructions having a DIT less than the current (simulated) time are included in the Ready Set (column 8, lines 22-28). The DIT for an instruction is the latest time at which the instruction can be issued and still complete at the time it would have completed if it had been issued immediately (column 11, lines 21-24). Instructions in the Ready Set are then scheduled in order of their cost (column 11, lines 36-38).

Rasbold thus differs significantly from Applicants' invention.

A. Rasbold Schedules Instructions Based on Cost, Not on the Basis of Whether the Instructions Add or Remove Elements from a Memory Queue

As described above, after a Ready Set is populated with instructions in Rasbold, the instructions are scheduled in order of their cost. The cost is defined as "the execution time of the instruction plus the cumulative execution times of all other instructions which depend therefrom" (column 9, lines 36-39).

In contrast, in embodiments of the present invention, instructions are removed from a Ready Set based on their impact on a memory queue. In particular, the desire is to keep the memory queue filled as close to a threshold level as possible (page 7, lines 4-11). The threshold depends on the processor that services the queue; an example threshold is one entry less than full, in order to keep the processor from stalling.

Thus, Rasbold is significantly different from Applicants' invention in regard to how or when instructions are removed from a Ready Set.

V. Selected Claims

A. Claims 1-7

Claim 1 has been amended to more clearly indicate that instructions in a ready set are removed on the basis of their impact on a memory queue – whether they add elements to a

memory queue or remove elements from the queue. As described in Section IV.A, Rasbold schedules instructions based on their cost.

Claim 3 was cancelled.

B. Claims 8-14

Claim 8 has been amended to more clearly indicate that instructions in a ready set are removed on the basis of their impact on a memory queue – whether they add elements to a memory queue or remove elements from the queue. As described in Section IV.A, Rasbold schedules instructions based on their cost.

Claim 10 was cancelled.

C. Claims 15-18

Claim 15 has been amended to more clearly indicate that instructions in a ready set are queued on the basis of their effect on memory operations – e.g., whether they add elements to a memory queue or remove elements from the queue. As described in Section IV.A, Rasbold schedules instructions based on their cost.

In particular, claim 15 recites:

-- a ready set evaluation module configured to evaluate instructions for their effect on memory operations; and

-- a code scheduling module configured to determine a desirable number of elements for a queue and choose an instruction node that will adjust the number of elements in the queue accordingly.

D. Claims 19-20

Claims 19-20 are new.

CONCLUSION

No new matter has been added with the preceding amendments. It is submitted that the application is in suitable condition for allowance. Such action is respectfully requested. If prosecution of this application may be facilitated through a telephone interview, the Examiner is invited to contact Applicant's attorney identified below.

Respectfully submitted,

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